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EXAMINER
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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/632,089  
Filing Date: August 01, 2003  
Appellant(s): TIRKKONEN ET AL.

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Majid S. AlBassam  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 2/23/07 appealing from the Office action  
mailed 6/20/06.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

20010055332	Sadjadpour et al	1-2001
20030128769	Kim	1-2003

Applicant's admitted prior art, Figures 1-2 and paragraphs [0005] through [0023], hereafter AAPA.

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims **1, 18, 23** are rejected under 35 U.S.C. 102(a) as being anticipated by **Sadjadpour et al** (US 2001/0055332).

Regarding claim **1**, **Sadjadpour** discloses a communication system for transferring data between a transmitter and a receiver over a plurality of channels, the communication system comprising:

- modulation circuitry having a plurality of modulation alphabets providing a set of bit loading sequences (see [0027]);
- circuitry for determining a power allocation for at least one bit loading sequence based on minimizing an error rate (see Fig. 6, and [0038], [0043] through [0048])

regarding the function 62 for minimizing bit-error-rate BER for the bit and power allocation algorithm, block 73 in Fig. 6); and

- circuitry for selecting a bit loading sequence with a lowest error rate (see [0038], [0044], [0045] regarding the function 62 in Fig. 6 for minimizing BER).

Regarding claims **18, 23**, the claims are interpreted and rejected for the same reason as set forth in claim 1 above.

2. Claims **2-13, 19-20, 22** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Sadjadpour** in view of Applicant's admitted prior art (Fig. 1-2 and [0005]-[0023]), hereafter, AAPA.

Regarding claim **2**, **Sadjadpour** would disclose all the claimed limitations, see claim 1 above, except for a multiple-input multiple-output (MIMO) system. However, since **Sadjadpour** teaches a multi-carrier modulator (see [0027]), one skilled in the art would recognize that the method as taught by **Sadjadpour** would be applicable to the MIMO system in AAPA and would work equally well (i.e, reducing cross-talk in a wireless phone). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate **Sadjadpour's** teaching to the MIMO system in AAPA as well, thereby providing a MIMO system as claimed, for utilizing advantages of a wireless MIMO system such as eliminating a cable while improving throughput performance of a communication device (i.e, increase transmission capacity by utilizing multiple transmit and receive antennas).

Regarding claims **3-4, 9, 11-13**, the claims are rejected for the same reason as set forth in claim 2 above. In addition, it is clear that Sadjadpour as modified in view of AAPA, would disclose power weighting (see AAPA, Fig. 1, [0010]) and plurality of antennas (see AAPA, Fig. 1) and OFDM decomposed channels as claimed (see AAPA, [0013] through [0018], noting for “sub-channels” and “orthogonal beams”. See also Sadjadpour, [0033] regarding “weighted combination”, read on power weighting, and [0027] regarding “sub-bands”, read on “logical channels”).

Regarding claims **5-6**, the claims are rejected for the same reason as set forth in claim 2 above. In addition, it would have been obvious to provide a “fixed” data rate as suggested by **Sadjadpour** (see [0038]-[0039] regarding a “desired” data rate), for conforming to a network configuration.

Regarding claims **7-8**, the claims are rejected for the same reason as set forth in claim 2 above. In addition, **Sadjadpour** would disclose a channel quality is measured at the transmitter and receiver as claimed (see Sadjadpour [0029] regarding noise PSD measurement).

Regarding claim **10**, the claim is rejected for the same reason as set forth in claim 9 above. In addition, since one skilled in the art would recognize the need of increasing transmission power for weak channels in order to satisfy a minimum signal-to-noise ratio requirement for transmission, it would have been obvious to one skilled in the art at the time the invention was made to modify **Sadjadpour** for allocating greater power weighing to weaker channels as claimed, in order to meet a minimum channel quality requirement for transmission.

Regarding claims **19-20, 22**, the claims are interpreted and rejected for the same reason as set forth in claim 3 above. In addition, **Sadjadpour** as modified in view of AAPA, would disclose decomposing a communication channel into a plurality of logical channels (see AAPA, [0013-0018] regarding "sub-channels", **Sadjadpour** [0027] regarding "sub-bands").

3. Claims **14-17, 21** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Sadjadpour** in view of AAPA and further in view of **Kim et al** (2003/0128769).

Regarding claim **14**, the claim is rejected for the same reason as set forth in claim 1 above. In addition, since codings and modulations that utilize system bits and parity bits are well known in the art as disclosed by **Kim** (see Fig. 3 and [0076], [0077]), it would have been obvious to one skilled in the art at the time the invention was made to incorporate Kim's teaching to **Sadjadpour** for coding data into a plurality of modulation schemes utilizing system bits and parity bits as claimed, in order to provide a suitable modulation and coding scheme in accordance with the channel quality condition (Kim's motivation).

Regarding claim **15**, the claim is rejected for the same reason as set forth in claim 14 above. In addition, **Sadjadpour** as modified would disclose the parity bits are transferred on a weak channel (see **Kim**, [0104]).

Regarding claim **16**, the claim is rejected for the same reason as set forth in claim 15 above. In addition, **Sadjadpour** as modified would disclose the parity bits are

transferred on a weak channel (see **Kim**, [0104]) and the power allocation is reduced (see **Kim**, [0098] regarding more transmission power to a good channel).

Regarding claim 17, the claim is rejected for the same reason as set forth in claim 15 above. In addition, as disclosed by **Kim**, a modulation scheme for a good channel condition would either comprise only systematic bits or a combination of systematic bits and parity bits (see Fig. 3, [0076], [0077]). Therefore, when a combination of systematic bits and parity bits is used for interleavers, the parity bits would be transferred in a least significant bits as claimed (this is a common way for interleaving systematic bits and parity bits, wherein the systematic bits would be transferred in a most significant bits).

Regarding claim 21, the claim is rejected for the same reason as set forth in claim 15 above.

## **(10) Response to Argument**

### **Claim 1**

In the appeal brief, pages 8-10, Appellants argue that

The Office Action took the position that Sadjadpour disclosed, at paragraphs 0043-0046, modulation circuitry having a plurality of modulation alphabets providing a set of bit loading sequences, circuitry configured to determine power allocation for at least one bit loading sequence based on minimizing an error rate, and circuitry configured to select a bit loading sequence with a lowest error rate, as recited in Appellants' claim 1. However, Appellants respectfully submit that no such disclosure exists in Sadjadpour. Paragraphs 0043-0046 of Sadjadpour are directed to Figure 6 thereof, and they are directed to blocks 61-68 representing various objective functions that can be identified from various algorithms. Function 64 is directed to representing minimization of an arbitrary function of total power and maximization of total data rate. Block 61 of Sadjadpour illustrates functions which can apply joined minimization of the cross talk and maximization of the total data rate. A further discussion of this aspect of Sadjadpour can be found in paragraphs 39-42 thereof.

Therefore, Sadjadpour only discloses selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk. Sadjadpour, however, fails to disclose or suggest circuitry configured to select a bit

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loading sequence with the lowest error rate. Appellants respectfully submit that there is simply no disclosure or suggestion in Sadjadpour of any elements which could be comparable to the circuitry as recited in claim 1, wherein a power allocation is determined for at least one bit loading sequence based on minimizing an error rate. As discussed above, and as discussed in Appellants' previous responses, the present invention is directed to a device which contains circuitry and which can perform a step of selecting a bit loading sequence based on a lowest error rate.

Furthermore, Appellants submit that Sadjadpour fails to teach or suggest "circuitry configured to determine a power allocation for at least one bit loading sequence based on minimizing an error rate," as recited in claim 1. As noted above, Sadjadpour does not teach or disclose power allocation for bit loading frequencies based on minimizing the error rate; rather, Sadjadpour discloses only power allocation based only on reducing the cross talk. There is no teaching or suggestion in Sadjadpour of power allocation for bit loading frequencies based on minimizing the error rate, and as such, Appellants submit that it is incorrect for the final Office Action to suggest or conclude, without specific citation to the prior art, that Sadjadpour teaches power allocation for bit loading frequencies based on minimizing the error rate when only cross talk is discussed in Sadjadpour.

For at least the reasons discussed above, Appellants submit that Sadjadpour fails to disclose or suggest all of the elements of claim 1. Accordingly, the Board's consideration and reversal of the rejection thereof is respectfully requested.

In response, it is noted that although the Examiner has specifically pointed out the function **62** in previous responses (Final Office Action and Advisory Action) regarding the BER minimization of the function **62** in Fig. 6 for the rejection, this function **62** is **never** mentioned by Appellants in his/her arguments through out the prosecution of this application, instead, only functions **61** and **64** are specifically mentioned by Appellants. Accordingly, Examiner assumes that Appellants have intentionally ignored Examiner's arguments and fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

In fact, since Sadjadpour does teach a bit and power allocation algorithm (see Fig. 6, block 73) for a selected function to be optimized (see [0045], [0046], noting that any function 61-68 in Fig. 6 can be selected for inputting to the bit and power allocation

algorithm 73), and since the function 62 that minimizes the bit-error-rate BER (see [0044] regarding function 62) can be selected for optimizing, it is clear that Sadjadpour would teach a bit loading and power allocation algorithm for minimizing BER according to the constraints of function 62 (see [0038], [0041]). By minimizing BER, it is clear that the lowest BER is selected. Here, although function 62 provides a joint minimization of the BER and maximization of the total data rate, the BER minimization criteria for bit loading and power allocation algorithm would read on the claimed limitation

“circuitry for determining a power allocation for at least one bit loading sequence based on minimizing an error rate; and

circuitry for selecting a bit loading sequence with a lowest error rate”.

Also note that since Sadjadpour does teach that the bit allocation algorithm and power allocation needed are re-calculated and re-sorted (see [0038]), it is clear that there is variability of the power allocation of the selected bit loading in order to minimize an error rate, as recited in Appellants' claims.

### **Claim 18**

Again, only functions **61** and **64** are specifically mentioned by Appellants in arguments (pages 11-12). Accordingly, Examiner assumes that Appellants have intentionally ignored Examiner's rejections and arguments regarding function 62 in Fig. 6, and fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

In fact, since Sadjadpour does teach a bit and power allocation algorithm (see Fig. 6, block 73) for a selected function to be optimized (see [0045], [0046], noting that any function 61-68 in Fig. 6 can be selected for inputting to the bit and power allocation algorithm), and since the function 62 that minimizes the bit-error-rate BER (see [0044] regarding function 62) can be selected for optimizing, it is clear that Sadjadpour would teach a bit loading and power allocation algorithm for minimizing BER according to the constraints of function 62 (see [0038], [0041]). By minimizing BER, it is clear that the lowest BER is selected. Here, although function 62 provides a joint minimization of the BER and maximization of the total data rate, the BER minimization criteria for bit loading and power allocation algorithm would read on the claimed limitation

“circuitry for determining a power allocation for at least one bit loading sequence based on minimizing an error rate; and  
circuitry for selecting a bit loading sequence with a lowest error rate”.

### **Claim 23**

Again, only functions 61 and 64 are specifically mentioned by Appellants in arguments (pages 14-15). Accordingly, Examiner assumes that Appellants have intentionally ignored Examiner's rejections and arguments regarding function 62 in Fig. 6, and fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

In fact, since Sadjadpour does teach a bit and power allocation algorithm (see Fig. 6, block 73) for a selected function to be optimized (see [0045], [0046], noting that any function 61-68 in Fig. 6 can be selected for inputting to the bit and power allocation algorithm), and since the function 62 that minimizes the bit-error-rate BER (see [0044] regarding function 62) can be selected for optimizing, it is clear that Sadjadpour would teach a bit loading and power allocation algorithm for minimizing BER according to the constraints of function 62 (see [0038], [0041]). By minimizing BER, it is clear that the lowest BER is selected. Here, although function 62 provides a joint minimization of the BER and maximization of the total data rate, the BER minimization criteria for bit loading and power allocation algorithm would read on the claimed limitation

“circuitry for determining a power allocation for at least one bit loading sequence based on minimizing an error rate; and

circuitry for selecting a bit loading sequence with a lowest error rate”.

### **Claims 2-13**

Since the arguments for claims 2-13 (pages 16-19) are all relying on the patentability of claim 1, the same response would be applied for the same reason as set forth in claim 1 above.

### **Claim 19**

Since the arguments rely on the patentability of “a third circuitry for choosing a bit loading sequence having a minimum error rate” (page 21), the same response would be

applied for the same reason as set forth in claim 1 above. Note that the bit loading and power allocation algorithm in Sadjadpour would implicitly comprise claimed circuitries in order to modulate and encode data (bit loading), and allocate power for transmission.

### **Claim 20**

On pages 23-24, Appellants argue that

Sadjadpour does not teach or disclose allocating power weighting to a logical channel for minimizing a bit error rate of a corresponding bit loading sequence and choosing at least one bit loading sequence based on minimizing an error rate, as recited in claim 20. As discussed above, Sadjadpour only discloses selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk. Sadjadpour, however, fails to disclose or suggest allocating a power weighting to the corresponding logical channel for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences and choosing a bit loading sequence having a minimum bit error rate. Appellants respectfully submit that there is simply no disclosure or suggestion in Sadjadpour of any elements which could be comparable to the allocating and choosing steps recited in claim 20, wherein a power allocation is determined for at least one bit loading sequence based on minimizing an error rate.

Further, Appellants submit that the cited portions of Appellants' specification (paragraphs [0005]-[0023]) also do not teach, show, or suggest the limitations recited in claim 20. More particularly, Appellants submit that AAPA does not teach allocating power weighting to a logical channel for minimizing a bit error rate of a corresponding bit loading sequence and choosing at least one bit loading sequence based on minimizing an error rate. As such, Appellants submit that AAPA does not further the teaching of Sadjadpour to the level necessary to properly support an obviousness rejection of claim 20.

In response, the examiner asserts that the sub-bands of QAM channels in Sadjadpour ([0027]), or the independent sub-channels in AAPA ([0013]) would read on the claimed "logical channels", the "weighted combination" in Sadjadpour ([0033]), or the "weighting unit" in AAPA (Fig. 1, [0010]) would read on the claimed "power weighting", the BER minimization criteria of the select function **62, 69** for bit loading and power allocation algorithm **73** in Fig. 6 of Sadjadpour would read on the claimed limitation "minimizing a bit error rate of a corresponding bit loading sequence and

choosing at least one bit loading sequence based on minimizing an error rate", as recited in claim 20.

### **Claim 22**

Since the arguments for the patentability of claim 22 (page 25) are similar to those of the patentability of claim 20, the same response would be applied for the same reason as set forth in claim 20 above.

In addition, on page 26, Appellants further argue that

With regard to each of the obviousness rejections discussed above, Appellants submit that in addition to the above noted remarks, Appellants further note that the method shown in the description of Sadjadpour is specifically related to the problem of cross talk in twisted pair modems, and as such, the method of Sadjadpour describes a weighting algorithm to reduce cross talk based on twisted pair cross talk algorithms. Appellants note that even if a person of skill in the art were to examine the teaching of Sadjadpour, they would not have considered Sadjadpour to be a suitable starting point for generating Appellants' claimed invention, as fields of wired and wireless communication are significantly different in most aspects. Appellants submit that one of skill in the art working in a twisted pair environment would not look to a wireless solution to solve a twisted pair problem. Thus, Appellants submit that in the absence of any teaching, suggestion, or motivation to do so found in the references themselves, a person skilled in the art would not have considered modifying a twisted pair modem communication technique for application in a wireless communication system, and combination of such teachings is references cited in support of the inappropriate. Thus, Appellants submit that the §103 rejection are not properly combined, and reconsideration and withdrawal of the obviousness rejections is respectfully requested.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, since Sadjadpour

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and AAPA **both** direct to a communication device (i.e, a phone), a bit and power allocation algorithm (voice coding), and since one skilled in the art would recognize that the voice coding (or bit and power allocation) algorithm would apply and work equally well for both wired phones and wireless phones, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Sadjadpour's teaching to a wireless system for reducing cross-talk in a wireless phone as well, while utilizing advantages of a wireless system such as eliminating a cable. The "fields of wired and wireless communication are significantly different in most aspects" as alleged by Appellants (page 26) is believed to be most in the field of switching/routing a call (i.e, handoff a call from one base station to another base station due to movements of wireless phones).

For foregoing reasons, the combination of Sadjadpour and AAPA is proper.

### **Claims 14-17 and 21**

On pages 27-28, Appellants argue that

Sadjadpour and AAPA are discussed above. Kim discloses a method for providing first and second interleaved bit streams to a modulator in order to transmit the first and second interleaved bit streams through at least two antennas in a mobile communication system. An encoder encodes a transmission data stream into a first bit stream with first priority and a second bit stream with second priority being lower than the first priority. An interleaver interleaves the first and second bit streams into the first and second interleaved bit streams. The modulator modulates the first and second interleaved bit streams.

Appellants respectfully submit that the combination of Sadjadpour, AAPA, and Kim fails to disclose or suggest all of the elements of claims 14-17 and 21. In rejecting claims under 35 USC §103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. In re Fine, 837 F.2d 1071,1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In doing so, the PTO is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966), and to provide a reason why one of ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reasons must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. F-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d

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1434, 1438 (Fed. Cir. 1988), cert. denied, 488 U.S.825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929,933 (Fed. Cir. 1984). These showings by the PTO are an essential part of complying with the burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Further, to establish prima facie obviousness of a claimed invention, all the claimed limitations must be suggested or taught by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1970). All words in a claim must be considered in judging the patentability of that claim against the prior art. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If the PTO fails to meet this burden, the Applicant is entitled to a patent. In re Glaug, 62 USPQ2d 1151 (Fed. Cir. 2002). In the present case, discussed in detail below, Appellants respectfully submit the PTO has failed to meet this burden.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, since Sadjadpour, AAPA and Kim **all** direct to a modulation and encoding technique, and since one skilled in the art would recognize that interleaving systematic bits and parity bits is just a well known feature of the modulation and encoding technique, the combination is proper. Here, Kim is used for a well known feature of the interleaver that both Sadjadpour and AAPA would implicitly teach in the bit and power allocation algorithm but are silent about it (note for the interleaving component in coding unit 12 of Fig. 1 in AAPA). Further, since Kim teaches a particular interleaving method according to channel conditions in a MIMO system, it would have been obvious to one

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skilled in the art at the time the invention was made to incorporate Kim's teaching to further improve the performance of the MIMO system as well.

For foregoing reasons, the combination is proper.

**Claims 14-17**

Since the arguments for claims 14-17 (pages 29-30) are all relying on the patentability of claim 1, the same response would be applied for the same reason as set forth in claim 1 above.

**Claim 21**

Since the arguments (page 30) rely on the patentability of claim 20, the same response would be applied for the same reason as set forth in claim 20 above.

**(11) Related Proceeding(s) Appendix**


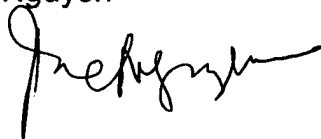
No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

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For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Duc Nguyen



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